NVIDIA

NVIDIA JETSON TX1 PCIe COMPLIANCE TESTING REFERENCE

DA-09103-001_v1.0 | August 2018

Application Note

DOCUMENT CHANGE HISTORY

DA-09103-001_v1.0

Version	Date	Description of Change
1.0	August 22, 2018	Initial Release

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OVERVIEW

NVIDIA® Jetson™ TX1 includes the Peripheral Component Interconnect Express (PCIe) interface. The implementation in Jetson TX1 supports both 2.5 G (PCIe Gen1) and 5.0 G (PCIe Gen2) transfer rates.

This application note describes the test equipment, software, and setup required to run the PCI Express (PCIe) Gen1 and Gen2 electrical compliance tests. The Jetson TX1 has been tested under worst case scenarios and the hardware can adapt to the compliant devices and channel automatically. The hardware calibrates the termination impedance for both PCIe transmitter and receiver, and the receiver adapts its internal parameters to optimize signal characteristics. The hardware is designed to directly work with compliant devices and compliant channels automatically. Therefore, no tuning will be required if customer designs follow the routing guidelines published in our design guide.

The lane mappings for the configurations are internal to the PCIe root port controller. For the supported configurations, refer to the OEM product design guide for Jetson TX1.

EQUIPMENT

The components required to perform PCIe compliance testing include:

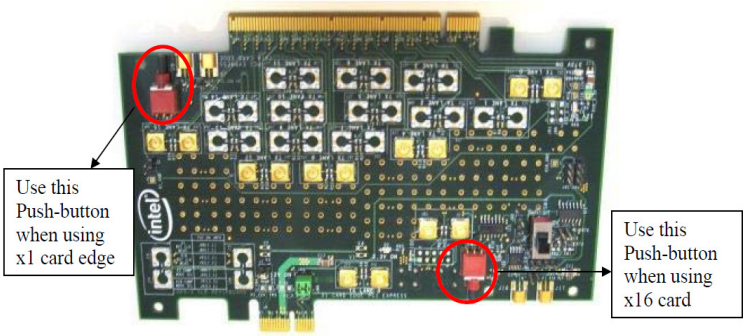
- Test Fixture
- Oscilloscope
- Probe
- Cables
- Termination Load/Adapter
- Software
  - PCI-SIG Clock Jitter Tool
  - SigTest 3.2.0

There are many tools currently available to help with compliance testing. The following sections list some of the equipment available. Items marked with an asterisk (*) indicate equipment that NVIDIA has used in its testing.

TEST FIXTURES

Test fixtures are used to connect the probes to the **TX** pins of the PCIe interface. Fixtures of different interface types are available and are recommended over using adapters to convert the interface type. Whichever fixture is selected, it must have SMP interconnects to avoid impedance mismatches due to discontinuities.

Table 1. Partial List of PCIe Test Fixtures

Product	Image and Description
PCIe Gen2 CLB v2 (for desktop CEM) See Note	

Notes:

CLB is Revision 2.0 Compliance Board.

There are two different versions of CLB:

- x1/x16 which has x1 and x16 card edges for testing x1 and x16 motherboard slots
- x4/x8 which has x4 and x8 card edges for testing x4 and x8 motherboard slots

The compliance load board (CLB) version(s) needed for testing a motherboard depend on the slot widths on the motherboard. All slots on the motherboard must be tested. Ordering information for the CLB can be found on PCI-SIG website at: http://pcisig.com/pci-express-compliance-load-board-clb

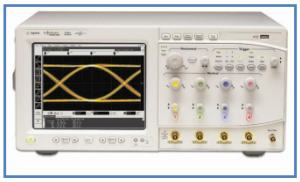
OSCILLOSCOPE

An oscilloscope is used to measure the signals.

PCIe Gen1

For PCIe Gen1, the PCIe specification requires that the oscilloscope have at least 6 GHz of bandwidth.

Table 2. Partial List of Instruments for PCIe Gen1

Company	Product	Image and Description
Tektronix*	TDS6604B or better	
Agilent	DSO/DSA91304A or better	

PCIe Gen2

For PCIe Gen2, the PCIe specification requires that the oscilloscope have at least 12 GHz of bandwidth.

Table 3. Partial List of Instruments for PCIe Gen2

Company	Product	Image and Description
Tektronix*	DSA71254 or better	
Agilent	DSO81304B or better	

PROBES

Probes are used to connect the oscilloscope to the test fixture; oscilloscope probes must be a minimum of 8 GHz of bandwidth.

Table 4. Partial List of Probes

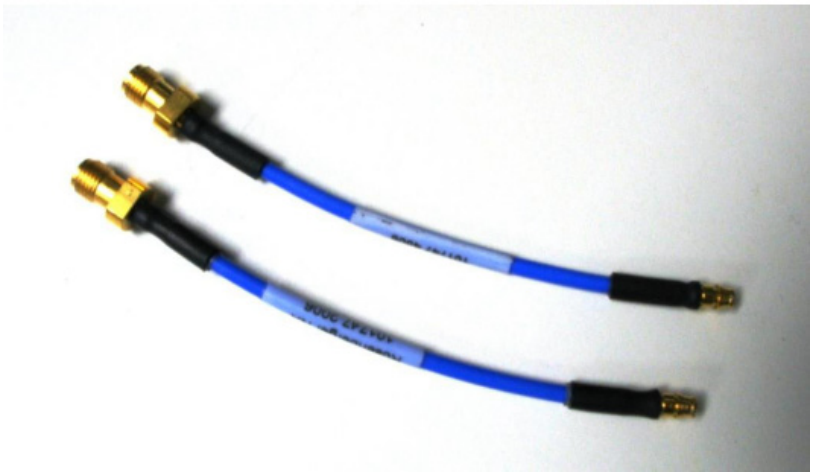
Company	Product	Image and Description
Tektronix*	1169A Requires Agilent N5380A	

CABLES

Cables are used to measure signal quality.

Table 5. Partial List of Cables

Company	Product	Image and Description
Tektronix*	174-4944-xx Two pairs of matched SMA-SMA cables (skew <1ps)	

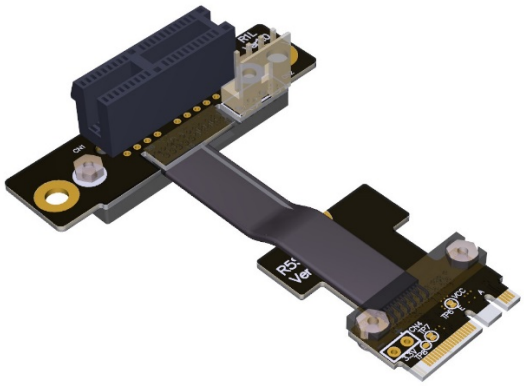
Company	Product	Image and Description
Pasternack*	P/N PE9514, Two pairs matched SMA-SMP adapters	
Tektronix*	Two pairs matched SMA-SMP cables	

TERMINATION LOAD/ADAPTER

The following table is a list of termination load/adapters.

Table 6. Partial List of Termination Load/Adapter

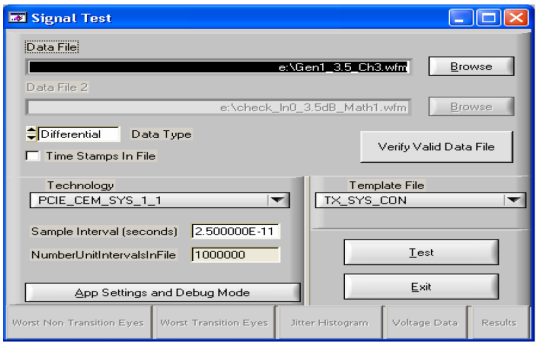
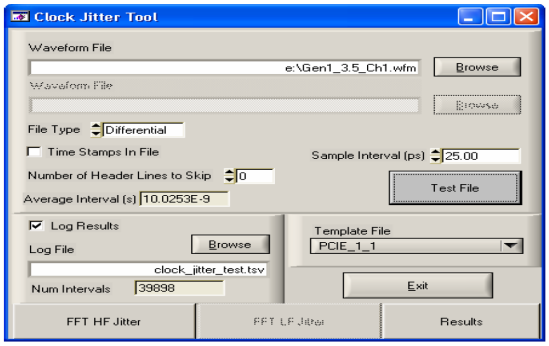
Product	Image and Description
50 Ohm Termination Load*	

Product	Image and Description
PCIe convert to M.2 Key E adapter	

SOFTWARE

Use of official compliance test software is recommended, but not required. While manually measuring the signal might be just as effective, it must ultimately pass with the compliance software at the compliance house.

Table 7. Recommended Test Software

Company	Product	Image and Description
PCI-SIG	SIGTEST 3 2.0	SIGTEST post processing analysis tool (version 3.2.0 or later): http://pcisig.com/developers/compliance-program 
PCI-SIG	Clock Jitter Tool 1.3.0	Clock Jitter Tool (version 1.3.0 or later): http://pcisig.com/developers/compliance-program 

SETUP EXAMPLE

The following figure is an example of a testing setup.

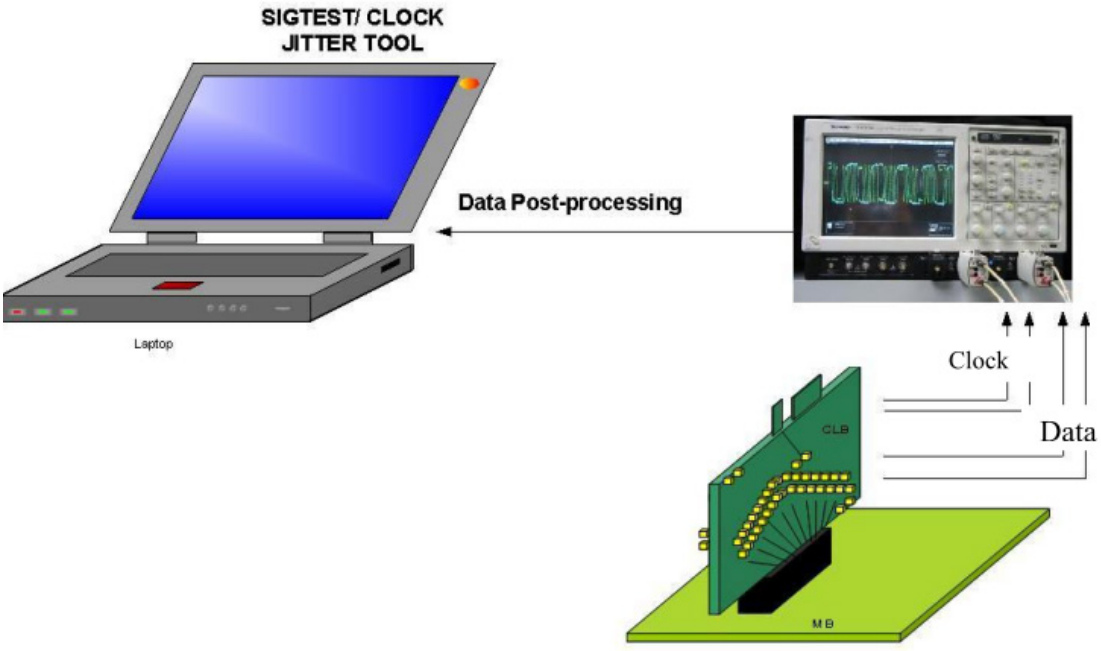


Figure 1. Setup Example

Notes:

1. Post processing tools Sigtest and Clock Jitter Tool can also be run on the scope.
2. Problem with reference. If system shows “in Error! Reference source not found.” Both reference clock and data lane under test must both be sampled simultaneously to carry out measurements as described in the *PCI Express Card Electromechanical Specification Revision 2.0*.

CEM 2.0 MEASUREMENTS USING TEKTRONIX SCOPE TDS61X4C

PCI-SIG provides the compliance standards and test descriptions for system boards and add-in cards that comply with *PCI Express Card Electromechanical Specification Revision 2.0*. Customers should refer to the document for an overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

PCI Express specification require devices to have a built-in mechanism for testing the electrical characteristics. Therefore, when the transmit lanes of the device are terminated with a 50-ohm load, the transmit lanes will automatically be forced into compliance mode.

DEBUGGING

High speed I/O design is difficult to debug and will get harder as speeds increase. The following are a few common PCI Express issues.

IF PCI EXPRESS DOES NOT WORK

If PCI Express does not respond or no signals are being sent out, verify the following:

1. Check the applied power for expected value.
2. Check that clocks are on.
3. Check for chip reset de-assertion.
4. Check the power sequencing.

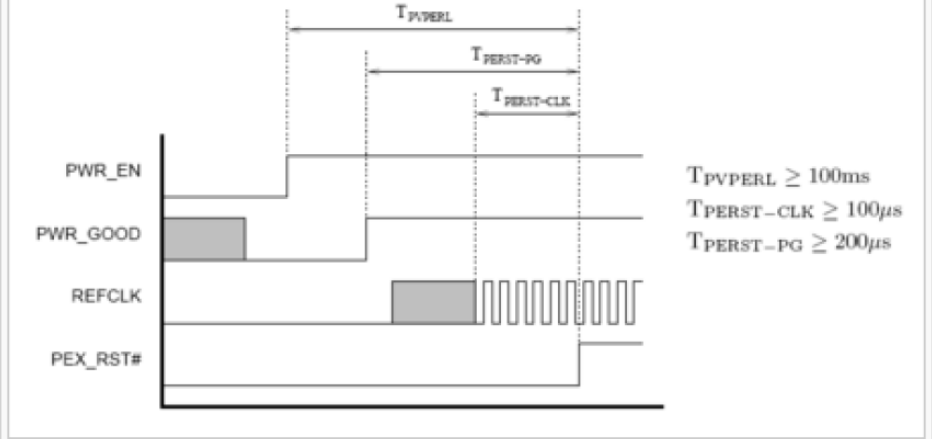


Figure 2. Power Sequence Diagram

DEVICE FAILS AT ASPM L0/L1 ENABLED

Connect device to a PCIe bus analyzer (for example, LeCroy Protocol Analyzer) to assist with the debug.

1. Configure analyzer to trigger on root repeatedly sending PM_Request_Ack DLLPs.
2. Capture the bus traffic at the time the bus failure occurs.